REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-15 are pending. Claims 1-15 stand rejected.

Claims 1, 4, 6, 9, 11 and 14 have been amended. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 112

The Examiner has rejected claim 5 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. The Examiner has stated that

> Claim 5 recites the limitation "the external alias" in lines 4 and 5. There is insufficient antecedent basis for this limitation in the claim. An "external alias" had not been previously cited.

(p. 2, Office Action 1/29/04)

Applicants respectfully submit that claim 5 contains antecedent basis for the claimed limitation in the preamble.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-3, 5-8 and 11-13 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,480,948 of Virajpet, et al. ("Virajpet") in view of U.S. Patent No. 6,240,519 of James, Jr., et al. ("James, Jr.") and U.S. Patent No. 6,567,093 of Tai, et al. ("Tai"). Claim 5 has been rejected according to the best possible interpretation in light of the 35 U.S.C. 112, second paragraph rejection. The Examiner has stated that

> Regarding claims 1, 6 and 11, Virajpet, et al. teaches a system for memory aliasing system. The processor is able to read from an internal R OM (memory) (31) for initialization (configuration) or boot code processing (col. 3, lines 1-16; col. 4, lines 5-

> 23). Section (31) of the memory map is configurable, and during a first period, the configurable section is aliased so that when the processor attempts to access this section (internal ROM), the access is directed toward the external ROM (20) under control of the bus/memory controller. Thus, when the processor seeks to address 00000000h, the access is directed toward an external non-volatile memory.

(p. 3, Office Action 1/29/04)

> Virajpet discloses
>
> Referring to FIG. 2, two memory maps for the computer system of FIG. 1 are shown. In both memory maps, a subset or section of addresses are set aside for each of the devices of the computer system. For example, sections of addresses are assigned to internal and external ROM while sections of addresses are assigned to internal and external RAM. A first section 31 of the memory map (e.g., the lowest addresses of the memory space) is configurable. Accordingly, during a first time period (e.g., after reset), the configurable section is aliased so that when processor 10 seeks to access to this section, the access actually occurs to internal ROM (e.g., element 18) and/or external ROM (e.g., element 20) under the control of the bus/memory controller 12. Thus, after reset, when processor 10 seeks to access address 00000000 (hex), the access will be directed to non-volatile memory (e.g., ROM) that is presumably unaffected by a reset condition.

(Col. 3, lines 1-16)

> According to an alternative embodiment of the present invention, the bus/memory controller 12 can access either the internal ROM or the external ROM upon reset. This can be achieved through pin strapping a Select signal line to the controller 12. When the Select line is coupled to ground (e.g., a logical "0"), an access by processor 10 to address 00000000(hex) will cause an access to an external memory such as external memory 20 for the initialization or boot code. If the Select line is set to a logical "1" (either by connecting it to a voltage source or leaving it unconnected in some situations), an access to address 00000000(hex) by the processor 10 will cause an access to an internal memory (e.g., internal ROM 18). As with the configurable memory map, the bus/memory controller controls the aliasing in this case. Use of the Select signal in this manner can be advantageous, for example, in that if there are changes that need to be made to the reset code instructions, those changes may be more easily made in external memory 20 compared to internal ROM 18.

(Col. 4, lines 5-23)

The Examiner has further stated that a difference between the claimed subject matter and Virajpet is the limitation of searching for a "valid secondary initialization routine." The Examiner states that such a limitation is disclosed in, and rendered obvious by James.

James, Jr. discloses

> Turning to FIGS. 6A-6D, illustrated is a flow chart of the boot block 202 code contained in the flash ROM 78. A start routine 500 consists of the power-up procedure of the system. The processor 32 first proceeds to the built-in self test (BIST) at step 505.

(Col. 7, lines 54-58)

> If the escape key was not pressed at step 525 during power up, then the processor 32 verifies the ROM 78 image at step 530. When the processor 32 verifies the ROM 78 image, the processor 32 determines whether the ROM 78 has become corrupt at step 535. If not, then the processor 32 proceeds to step 536, and executes the system block 208 code. However, if the ROM 78 image is corrupt, then the processor 32 continues to execute the boot block 202 code by proceeding to step 540 in FIG. 6B.

(Col. 8, lines 4-12)

> The processor 32 then unlocks the flash ROM 78 protection at step 630 and determines if a diskette is present in the floppy drive 74 at step 635. If no diskette is present, the processor then turns on the keyboard 68 LEDs 69, in accordance with the exemplary predefined prompt set, in step 637 before ending the procedure in step 665. The system must be reset to retry ROM flash. If a diskette is present, the processor locks the CMOS and Super I/O access at step 640. The processor 32 then issues audio beeps at step 645 and then performs a boot of the system at step 650. The boot is performed by issuing an INT 19 software interrupt. The boot is performed by the initialized floppy drive or ATAPI drive. At this point, the boot is of a minimal system whose purpose is to re-flash the flash ROM 78. So, after boot, the minimal system loads an executable for flashing the flash ROM 78, which is now unprotected.

(Col. 8, line 53 – Col. 9, line 1) (Emphasis added)

The Examiner has further stated that a difference between the claimed subject matter and Virajpet and James is the limitation of a configurable system-on-chip. The Examiner states that such a limitation is disclosed in, and rendered obvious by Tai.

Tai discloses

> ...system built in a single semiconductor chip, thereby lower cost, easier design, simpler mass production, relatively high operating speed, as well as less manufacturing failure rate can be realized.
>
> It must be noted that the semiconductor chip suggested by the present invention is not limited to the application in the field of CRT monitor. Actually it can be applied to any type of display system.

> The configuration of a system-on-chip according to the present invention is characterized by storing main program, DDC (display data channel) data, and DFF (display frame frequency) data together in a storage circuit such as a REPROM, and by a novel arrangement of connection between its storage circuit and its operating circuits such as a CPU, an interface unit, or a logic block.

(Col. 1, lines 45-60) (Emphasis added)

> ...video signal provider 22 or a system associated with the video signal provider 22. The single semiconductor chip 211 comprises:

(Col. 4, lines 44-46)

> The semiconductor chip 211 may further comprise a communication channel composed of, for example, a data bus 2113 and an address bus 2114, for the operating means 2112 to read the first group of data 2111d, the second group of data 2111f from storage means 2111, and to access the program 2111p from storage means 2111.
>
> The semiconductor chip 211 may have its operating means 2112 comprising a processing unit 2112P for reading the first group of data in response to the data request signal, and reading the corresponding part of second group of data according to the detected data mode. The processing unit 2112P may be similar to or the same as a conventional CPU (central processing unit) capable of executing the program 2111p and operating in accordance with the executed program.

(Col. 5, lines 16-30)

Applicants respectfully submit, however, that claim 1, as amended, is not obvious under 35 U.S.C. § 103 in view of Virajpet, James, Jr. and Tai. Claim 1 includes the following limitations.

> A method for multiple memory aliasing for a configurable system-on-a-chip, the configurable system on a chip integrating at least a central processing unit, an internal system bus, a programmable input/output, and a programmable logic, on a single integrated circuit device, the method comprising:
>
> executing code from a read-only memory (ROM) internal memory, said ROM internal memory having an alias;
>
> searching for a valid secondary initialization routine to configure the system including system peripherals;
>
> locating a configuration program in the ROM internal memory;
>
> disabling the ROM internal memory alias; and
>
> jumping to the secondary initialization routine located in a FLASH external memory.

(Claim 1) (emphasis added)

Applicants have amended claim 1 to clarify the nature of the secondary initialization routine. As claimed, the secondary initialization routine is used to configure the system including the peripherals. The secondary initialization routine is not used for the primary initialization, but for secondary initialization including peripherals.

In contrast, the floppy disk of James, which the Examiner equates with the external memory, performs a bare boot operation. The sole purpose of this operation is to provide the minimal operating system necessary to flash the ROM.

Applicants respectfully submit that there is a lack of motivation to combine Virajpet and James in the manner suggested by the Examiner. The configurable memory map disclosed in Virajpet does not benefit in any way from the provision and detection of a floppy disk containing a minimal boot operation as disclosed in James. That is, Virajpet is not at all concerned with a problematic flashing of a ROM, and therefore, does not benefit from providing a minimal operating system necessary to flash the ROM in an external device.

Additionally, applicants respectfully submit that the configurable system-on-chip, as claimed, cannot be equated with the single chip in Tai which is configured to better perform the video signal adapting functions typically effected by multiple chips. The system disclosed in Tai is not fully configurable. Applicants have amended the claim to clarify this distinction. The configurable system-on-chip, as claimed, contains a programmable input/output, not disclosed in any combination of the cited references.

For these reasons, applicants respectfully submit that claim 1 is not rendered obvious by any of Virajpet, James, Jr. or Tai, alone or in combination.

Given that claims 2 – 5 depend, directly or indirectly, from claim 1, applicants submit that claims 2 – 5 are, likewise, not obvious under §103 in view of the references cited by the Examiner. Further, given that claims 6 and 11 contain the limitations of a secondary

initialization routine used to configure the system including the peripherals and a configurable system-on-chip having a programmable input/output, and further given that claims 7 – 10, and claims 12 – 15 depend, directly or indirectly, from claims 6 and 11, respectively, applicants submit that claims 6 – 15 are, likewise, not obvious under §103 in view of the references cited by the Examiner.

Claims 4, 9, 10, 14 and 15 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,480,948 of Virajpet, et al. ("Virajpet") in view of U.S. Patent No. 6,240,519 of James, Jr., et al. ("James, Jr.") and U.S. Patent No. 6,567,093 of Tai, et al. ("Tai") as applied to the claims above, and further in view of U.S. Patent No. 6,401,164 of Bartoli, et al. ("Bartoli"). The Examiner has stated that

> The difference between the claimed subject matter of claims 4, 9, and 14 and that of Virajpet, et al, James, Jr., et al., and Tai, et al., disclosed supra, is that the claims recite that code is executed in a manner starting from the bottom of the ROM memory. Bartoli, et al. teaches both top and bottom boot sector configurations for an internal ROM device (Figures 1A & 1B; col. 1, line 49 – col. 2, line 19). Therefore, it would have been obvious to one of ordinary skill in the art having the teachings of Virajpet, et al., James, Jr., et al., Tai, et al., and Bartoli, et al. before him at the time the invention was made to modify the internal memory of Virajpet, et al., James, Jr., et al., and Tai, et al. to include reading initialization code from the top or bottom of the memory, because then greater functionality for specific system designs could be incorporated that would take advantage of reading from either the top or bottom of the internal memory for initialization routines.

(p. 5-6, Office Action 1/29/04)

Bartoli discloses

> FIGS. 1A and 1B respectively illustrate the differences between the top and bottom boot sector configurations in the above-mentioned example of a 4 Mbits word-organized Flash EEPROM. Such a memory has a size of 256 Kwords, and 18 address signals allow for individually addressing each memory location. Address signals A12-A17, that are a subset of the set of external address signals supplied to the memory device, are used for selecting one of the 11 memory sectors; an "X" in the tables of FIGS. 1A and 1B conventionally means a "don't care" logic state.
>
> Referring to FIG. 1A, wherein the boot sector is located at the top of the address space, the decoding scheme for address signals A12-A17 is the following: if the three most significant address signals A15-A17 are different from "111", then one of the seven sectors of 32 Kwords is addressed, depending on the particular logic configuration of

> signals A15-A17; address signals A12-A14, together with the remaining subset of twelve least significant external address signals A0-A11 (not shown in the drawing) are used for selecting a particular memory word among the 32 Kwords of the currently selected memory sector. If A15=A16=A17="1", then the boot sector is selected. To decide which of the four memory sectors of the boot sector is addressed, address signals A12-A14 are used. If A14="0", then the 16 Kwords sector is addressed, and A12, A13, together with A0-A11, are used to select one among the 16 Kwords. If differently A14="1", A13 is considered: if A13="1", then the 8 Kwords memory sector is addressed, and A12, together with A0-A11, is used to select one among the 8 Kwords. Finally, if A13="0", either one or the other of the two 4 Kwords memory sectors is addressed depending on A12 being "1" or "0"; A0-A11 are used to select one among the 4 Kwords of the selected sector.
>
> The situation in the case of a memory device with a boot sector located at the bottom of the address space, shown in FIG. 1B, is completely similar, the only difference being that the values of the address signals A12-A17 are the logic complements of those in FIG. 1A.

(Col. 1, line 49 – Col. 2, line 19)

> Assuming that the memory device is intended to be used in an electronic system wherein it is necessary that the boot sector is located at the top of the external address space, then during the memory device testing following its manufacturing...

(Col. 5, lines 12-16)

Applicants have amended the claims to clarify that the code is executed starting with the bottom of the external memory. Applicants respectfully submit that Bartoli does not disclose this limitation. Therefore, applicants respectfully submit that claims 4, 9, 10, 14, and 15 are not rendered obvious by the combination of Virajpet, James, Jr. and Tai and further in view of Bartoli.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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